A NEW POWER AMPLIFIER TOPOLOGY WITH SERIES BIASING AND POWER COMBINING OF TRANSISTORS

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ABSTRACT

A new power amplifier topology is described and demonstrated in a microwave monolithic integrated circuit (MMIC) implementation with GaAs MESFETs. This topology overcomes several limitations of the traditional approach of paralleling of power transistor unit cells. In the new topology, unit cells are both parallel and series combined. The benefits include higher input and output impedances, broadband power matched interstage networks, and high voltage biasing at reduced DC current.

INTRODUCTION

Traditionally, the common source/emitter configuration is used for microwave power amplifiers, with the device periphery determined by the desired maximum output power. In the case of the power MESFET, the layout consists of many unit gate fingers parallel connected to a common gate bus. The following example highlights some of the limitations of designing power MESFETs with this combining technique alone. Since gate attenuation increases with both frequency and unit finger width [1], unit finger widths are typically less than 200 microns in C-Band, and less than 75 microns in the Ku-band. Thus, for example, a 20 mm device in C-Band would require 100 unit gate fingers connected to the gate bus. Assuming a 40 micron gate finger spacing to limit the operating channel temperature [2] the gate bus of this device becomes 4 mm wide. The aspect ratio of this device is 20:1. The input impedance of such a device would be less than 0.5 Ohms, and the output less than 3 Ohms, requiring significant impedance transformation for matching. Furthermore, the drain bias network must support a drain current approaching 3 amps. To reduce the current requirements, series biasing of paralleled devices has been demonstrated [3]. However, this method does not affect device aspect ratio or the input and output matching impedances required for power operation. The topology described herein provides high voltage/low current operation, higher input and output impedances, simple broadband interstage power matching, and a reduced device aspect ratio for simplified matching networks.

THE NEW TOPOLOGY

The simplified circuit diagram shown in Figure 1 illustrates the new amplifier configuration. In this figure, all FETs are of equal size and the circuit elements are designed in such a way that each FET operates under the same DC and RF conditions. The B_i elements form a DC bias network to provide proper bias to the series connected FETs.

Table 1 compares some of the important DC and AC parameters between simple paralleling and the new series transistor configurations. In the latter approach, voltage is traded for current, for the same DC input power. Also, input and output impedances for the same total device size are N times and N^2 time higher, respectively. The series configuration has higher gain because a portion of the first FET's power output drives the gate of the second FET, and a portion of the second FET's output drives the gate of the third FET, and so on.

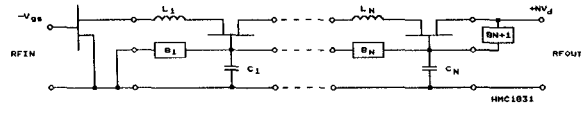

Figure 1. The new amplifier configuration.

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Parameter	Unit Cell	n Unit Cells Paralleled	n Unit Cells "Series" Connected
Periphery	W	nW	nW
Operating Current	½ I_{dss}	n/2 I_{dss}	½ I_{dss}
Operating Voltage	V_D	V_D	nV_D
C_{IN}	C_{gs}	nC_{gs}	C_{gs}
R_{OUT}	R_L	R_L/n	nR_L
Linear Gain	G	G	nG - (n-1)
P_{DC}	½ $I_{dss}V_D$	n/2 $I_{dss}V_D$	n/2 $I_{dss}V_D$
P_{RFIN}	P_i	nP_i	P_i
P_{RFOUT}	GP_i	nGP_i	nGP_i - (n-1)P_i
$\eta_{POWER\ ADDED}$	η_O	η_O	η_O

Table 1. Comparison of important parameters for simple paralleling and the new "series" transistor configuration.

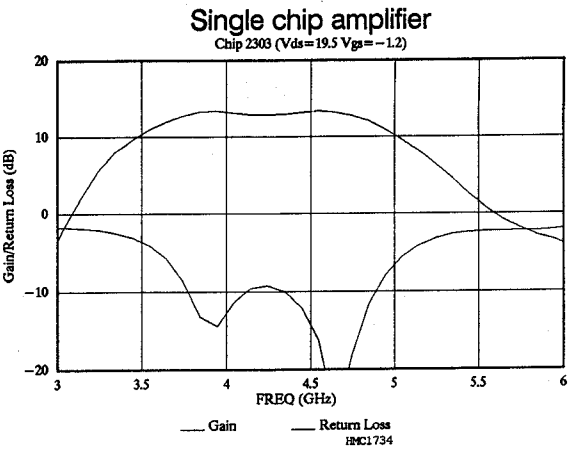

Figure 3. The 4 GHz single chip amplifier gain is approximately 13 dB over the 3.8 to 4.7 GHz frequency range. The worst case return loss over this range is 9 dB.

POWER AMPLIFIER MMIC

A fully monolithic 4 GHz power amplifier MMIC matched to 50 Ohms was designed using the new topology. A picture of the 3 mm by 4.4 mm chip is shown in Figure 2. The amplifier is composed of three 8 mm FETs combined in series for a total on chip periphery of 24 mm. The MMIC operates at 19.5 volts with a drain current of 1.2 amps. Small signal amplifier gain is 13 dB from 3.8 to 4.7 GHz with a return loss of better than 9 dB, as shown in Figure 3. The 1 dB gain compression power output from 4 to 5 GHz is 5 Watts with a chip level power added efficiency of 22% (Figure 4).

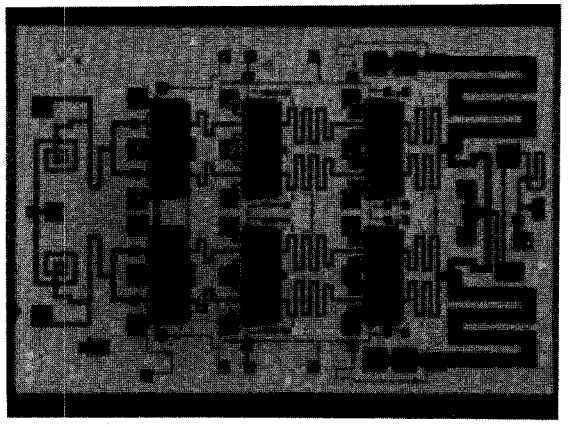

Figure 2. Chip photo of monolithic 4 GHz power amplifier designed using the new topology.

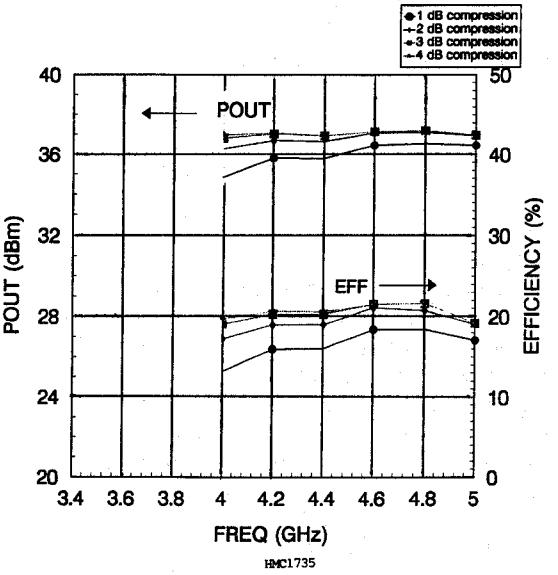

Figure 4. The 4 GHz single chip amplifier has a saturated power output of 37 dBm, and a power added efficiency greater than 20% from 4 to 5 GHz.

POWER AMPLIFIER HYBRID

The power MMIC provides a simple means of power combining since both input and output matching is contained on chip. A hybrid power amplifier consisting of four of the power MMICs has been fabricated and tested to demonstrate this feature. A photograph of the hybrid is shown in Figure 5. Power combining is accomplished

with Lange couplers and quarterwave (70 Ohm) transmission lines. The small signal gain varies from 12 to 13 dB between 3.7 and 4.6 GHz (Figure 6). The saturated output power is greater than 42 dBm from 3.7 to 4.8 GHz (Figure 7).

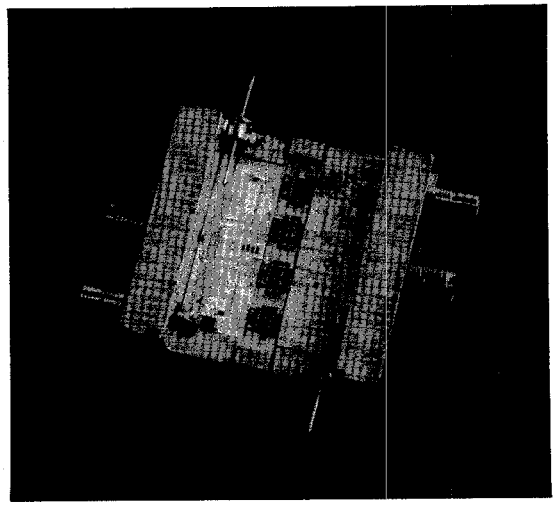

Figure 5. The power amplifier MMICs provide for simple power combining at the hybrid level since they are matched to 50 Ohms. This hybrid combines four of the MMICs.

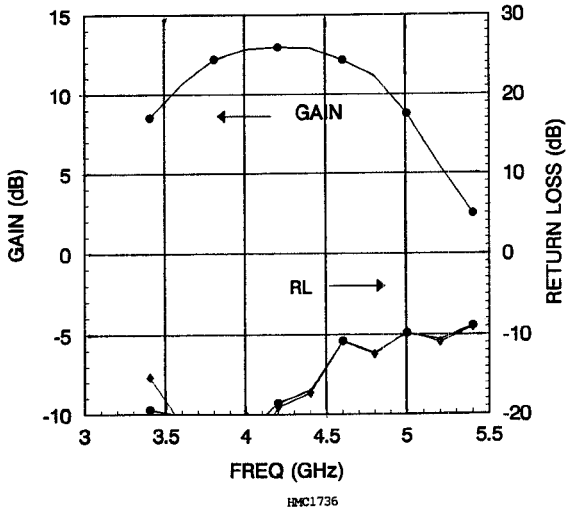

Figure 6. The hybrid amplifier has a small signal gain between 12 and 13 dB from 3.7 to 4.6 GHz.

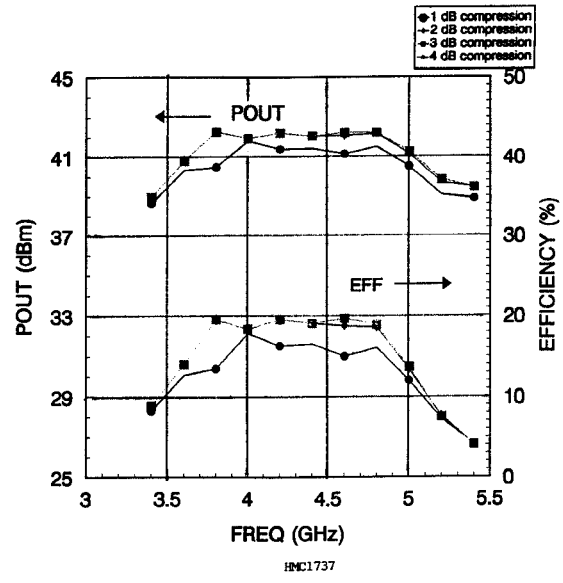

Figure 7. The hybrid amplifier has a saturated output power level of 42 dBm with a peak power added efficiency of 19%.

CONCLUSION

A new amplifier topology has been presented and described. This new topology provides solutions to several problems encountered when paralleling many unit gate cells to achieve large periphery power devices. The benefits include higher input and output impedances, high supply voltage/low current operation, low device aspect ratios, and low loss broadband power matched interstage networks. Measured results on a MMIC and a hybrid power amplifier implemented with this technique were also presented.

ACKNOWLEDGEMENTS

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